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Claim Amendments

Claims 1-49 (previously canceled).

50. (Currently amended) A high voltage field-effect transistor (HVFET) comprising:

a substrate of a first conductivity type;

a source [diffusion] region of a second conductivity type disposed in the substrate, the source [diffusion] region having a source fingertip area;

a first region of the second conductivity type disposed in the substrate, the first region having extended regions spaced-apart from the source [diffusion] region with [an IGFET] channel regions being formed therebetween, the first region [having a pair of drain fingertips areas] being inter-digitated with the source region [fingertip area];

a drain diffusion region of the second conductivity type disposed in the first region,

a buffer area of the first conductivity type [formed] between the source [diffusion] region and the first region [adjacent] proximate the source fingertip area, the buffer area being substantially wider than the [IGFET] channel regions;

an insulated gate disposed above the [IGFET] channel regions;

[at least one] a buried layer of the first conductivity type disposed within the first region, the [at least one] buried layer forming [two or more] upper and lower JFET channels in the first region.

51. (Original) The HVFET of claim 50 further comprising:

a drain electrode that includes a drain field plate which overlaps a portion of the first region.

52. (Original) The HVFET of claim 50 furth r comprising:

a source electrode that includes a source field plate which extends over the insulated gate.

53. (Original) The HVFET of claim 50 further comprising:

a tap diffusion region of the second conductivity type disposed in the first region near a perimeter boundary of the first region.

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54. (Currently amended) The HVFET according to claim 50 wherein the [at least one] buried layer [comprises a plurality of buried layers forming an associated plurality of JFET channels in the first region] is spaced-apart from the drain diffusion region.

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55. (Currently amended) The HVFET according to claim 50 further comprising:

a second [plurality of] buried layer[s] of the first conductivity type disposed beneath the source diffusion region.

56. (Currently amended) The HVFET according to claim 55 wherein the second [plurality of] buried layer[s] extends beneath the [IGFET] channel regions.

57. (Currently amended) The HVFET according to claim 50 wherein the [at least one] buried layer is connected to the substrate.

Claims 58-92 (previously canceled).

93. (Currently amended) A high voltage field-effect transistor (HVFET) comprising:

a substrate of a first conductivity type;

an epitaxial layer of a second conductivity type disposed on the substrate;

a diffusion region of the first conductivity type disposed in the epitaxial layer, a junction being formed between the diffusion region and the epitaxial layer;

a drain region of the second conductivity type disposed in the epitaxial layer and separated from the junction by a portion of the epitaxial layer;

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a source region of the second conductivity type disposed in the diffusion region, the source region being spaced-apart from the junction, a channel region being formed between the source region and the junction;

an insulated gate disposed above the channel region;

a buried layer of the first conductivity type disposed within the portion of the epitaxial layer, the buried layer being spaced-apart from the drain diffusion region, the buried layer acting as an effective gate to control [dual] current channels formed above and below the buried layer, the current channel formed above the buried layer having an impurity concentration of approximately 1 X $10^{12}/cm^2$.

94. (Original) The HVFET according to claim 93 wherein the buried layer is spaced-apart from the junction.

95. (Original) The HVFET according to claim 93 further comprising:

an additional buried layer of the first conductivity type disposed beneath the source region.

96. (Original) The HVFET according to claim 93 wherein the insulated gate extends laterally over the substrate from the source region to the buried layer.

97. (Original) The HVFET according to claim 96 wherein the insulated gate overlaps the buried layer.

98. (Original) The HVFET according to claim 93 wherein the buried layer extends beneath the drain region.

99. (Original) The HVFET according to claim 93 wherein the buried layer is connected to the substrate.

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100. (Original) The HVFET according to claim 93 wherein the first and second conductivity types are p-type and n-type, respectively.

101. (Original) The HVFET according to claim 93 further comprising:

a source electrode connected to the source region; and

a drain electrode connected to the drain region.

102. (Original) The HVFET according to claims 93, 94, 95, 96, 97, 98, 99, 100 or 101 further comprising:

an additional diffusion region of the first conductivity type disposed in the diffusion region adjacent the source region.

103. (Currently amended) A high voltage field-effect transistor (HVFET) comprising:

a substrate of a first conductivity type;

an epitaxial layer of a second conductivity type disposed on the substrate;

a drain diffusion region disposed in the epitaxial layer;

a first region of the first conductivity type disposed in th epitaxial layer;

a source diffusion region disposed in the first region spaced-apart from the epitaxial layer, an IGFET channel region being formed between the source diffusion region and the epitaxial layer;

a buried region of the first conductivity type disposed within the epitaxial layer, the buried region forming conduction channels within the epitaxial layer, one conduction channel being formed above the buried region with an impurity concentration of approximately 1 X $10^{12}/cm^2$ and another conduction channel being formed below the buried region, the buried region being spaced-apart from the drain diffusion region;

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an insulated gate formed above the IGFET channel region.

104. (Previously added) The HVFET according to claim 103 wherein the first region has a first surface that borders a surface of the epitaxial layer.

105. (Previously added) The HVFET according to claim 103 further comprising:

a second buried region of the first conductivity type disposed beneath the source diffusion region.

106. (Previously added) The HVFET according to claim 105 wherein the second buried region extends laterally under the IGFET channel region.

107. (Previously added) The HVFET according to claim 105 further comprising

a second region of the first conductivity type disposed in the first region adjacent to the source diffusion region.

108. (Previously added) The HVFET according to claim 103 wherein the buried region is connected to the substrate.

109. (Previously added) The HVFET according to claim 103 wherein the first and second conductivity types are p-type and n-type, respectively.

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110. (Previously added) The HVFET according to claim 103, further comprising:

a source electrode connected to the source diffusion region; and

a drain electrode connected to the drain diffusion region.

111. (Previously added) The HVFET according to claim 110 wherein the source and drain electrodes include field plate members.